CDX-C90R

SERVICE MANUAL

AEP Model
UK Model

Model Name Using Similar Mechanism	CDX-C780R
CD Drive Mechanism Type	MG-363S-121
Optical Pick-up Name	KSS-520A

SPECIFICATIONS

CD player section

System	Compact disc digital audio system
Signal-to-noise ratio	109 dB
Frequency response	5 - 20,000 Hz (±1 dB)
Wow and flutter	Below measurable limit
Laser Diode Properties	
Material	GaAlAs
Wavelength	780 nm
Emission Duration	Continuous
Laser output power	Less than 44.6 µW*

* *This output is the value measured at a distance of 200 mm from the objective lens surface on the Optical Pick-up Block.*

Tuner section

FM

Tuning range	87.5 - 108.0 MHz
Antenna terminal	External antenna connector
Intermediate frequency	10.7 MHz
Usable sensitivity	8 dBf
Selectivity	75 dB at 400 kHz
Signal-to-noise ratio	65 dB (stereo), 68 dB (mono)
Harmonic distortion at 1 kHz	0.3% (stereo), 0.3% (mono)
Separation	35 dB at 1 kHz
Frequency response	20 - 15,000 Hz

MW/LW

Tuning range	MW : 531 - 1,602 kHz LW : 153 - 281 kHz
Antenna terminal	External antenna connector
Intermediate frequency	10.71 MHz/450 kHz
Sensitivity	MW : 30 dBµV LW : 33 dBµV

General

Outputs	Digital output Line outputs (3) Power antenna relay control lead Power amplifier control lead Telephone ATT control lead Illumination control lead
Tone controls	Bass ±8 dB at 100 Hz Treble ±8 dB at 10 kHz
Power requirements	12 V DC car battery (negative ground)
Dimensions	Approx. 178 × 50 × 184 mm (w/h/d)
Mounting dimension	Approx. 182 × 53 × 163 mm (w/h/d)
Mass	Approx. 1.6 kg
Supplied accessories	Parts for installation and connections (1 set) Rotary remote RM-X90 (1) Wireless remote RM-X9R (1) Front panel case (1)

Design and specifications are subject to change without notice.

FM/MW/LW COMPACT DISC PLAYER

MICROFILM

SONY®

SECTION 3
DIAGRAMS

3-1. IC PIN DESCRIPTIONS

• IC5 CXP84640-011Q (CD SYSTEM CONTROL)

Pin No.	Pin Name	I/O	Pin Description
1 – 5	NCO	—	Not used in this set.
6	FP OPEN	I	Front panel open detection input
7	FP CLOSE	O	Front panel close control output
8	LINKOFF	I	Bus interface link input (Not used in this set.)
9	DRV OE	O	Focus/tracking coil/sled motor control output
10	$\overline{\text{D SW}}$	I	Down switch input (SW4)
11 – 13	NCO	—	Not used in this set.
14	LM EJ	O	Loading motor control output
15	LM LOD	O	Loading motor control output
16	EMPH O	O	De-emphasis ON/OFF control output
17	$\overline{\text{CDMON}}$	O	CD mechanism deck power control output
18	$\overline{\text{CD ON}}$	O	CD power control output
19	A MUT	O	System attenuate control output
20	$\overline{\text{LD ON}}$	O	Laser power ON/OFF control output
21	$\overline{\text{CD RST}}$	O	CD system reset output
22 – 24	—	—	Not used in this set.
25	PH3	I	Not used in this set.
26	TSTIN0	I	Not used in this set.
27	TSTIN1	I	Not used in this set.
28	$\overline{\text{TST CLV}}$	I	Not used in this set.
29	NCO	—	Not used in this set.
30	$\overline{\text{RESET}}$	I	System reset input (“L” = Reset)
31	$\overline{\text{X IN}}$	I	X’tal oscillator input of system clock. (10 MHz)
32	$\overline{\text{X OUT}}$	O	X’tal oscillator output of system clock. (10 MHz)
33	GND	—	Analog GND
34	$\overline{\text{XT OUT}}$	O	Not used in this set.
35	$\overline{\text{XT IN}}$	I	Not used in this set.
36	AVSS	—	A/D converter GND
37	AVREF	I	A/D converter reference voltage input
38	TEP L	I	Not used in this set.
39	TEP H	I	Not used in this set.
40	NCO	—	Not used in this set.
41	PH2	I	Not used in this set.
42	SCLK	O	CD-TEXT data read clock output
43	$\overline{\text{ESPXQOK}}$	O	XQOK signal output to DRAM controller.
44	ESPSDT	I	Serial data input from DRAM controller.
45	$\overline{\text{GRSRST}}$	O	Reset signal output to DRAM controller.
46	GRSCOR	I	Sub-cord sync input from DRAM controller.
47	CD XLAT	O	CD signal process serial latch output
48	TX CLK	O	EEPROM serial clock output
49	TX DATA	O	EEPROM serial data output
50	UNISO	O	Not used in this set.
51	BUS CLK	I/O	Bus system serial clock input/output
52	BUS SI	I	Bus system serial interface input
53	BUS SO	O	Bus system serial interface output
54	F OK	I	Focus OK signal input
55	GFS	I	GFS signal detection input
56	SCOR	O	Sub-cord sync output
57	SENS	I	SENS signal input
58	—	I	Fixed at “H” in this set.
59	CD CKO	O	CD signal process serial clock output

Pin No.	Pin Name	I/O	Pin Description
60	BU.IN	I	Back-up power detection input
61	$\overline{\text{BUSON}}$	I	Bus on control input
62	$\overline{\text{IN SW}}$	I	Disc in switch input (SW1)
63	$\overline{\text{SELF SW}}$	I	Self switch input (SW2)
64	$\overline{\text{TX CE}}$	O	EEPROM chip enable output
65	SCK2	O	Sub Q read clock output
66	SI2	I	Sub Q 80 bit, PCM peak and level data 16 bit input
67	CD DATA	O	CD signal process serial data output
68	$\overline{\text{ESPXWRE}}$	O	Write signal output to DRAM controller.
69	$\overline{\text{ESPXRDE}}$	O	Read signal output to DRAM controller.
70	$\overline{\text{ESPXLT}}$	O	Serial data latch output to DRAM controller.
71	$\overline{\text{ESPXSOE}}$	O	XSOE signal output to DRAM controller.
72	VDD	—	Power supply
73	HIN	I	Fixed at “H” in this set.
74	TEXT.ON/OFF	I	Fixed at “H” in this set.
75	PH1	I	Not used in this set.
76	FBTBSEL	I	Not used in this set.
77	$\overline{\text{CDOSEL}}$	I	Not used in this set.
78 – 80	—	—	Not used in this set.

• IC501 CXD2548R (DIGITAL SERVO, DIGITAL SIGNAL PROCESSOR)

Pin No.	Pin Name	I/O	Pin Description
1	SYSM	I	System mute input (Not used.)
2	RMUT1	O	R-ch, “0” detection output. (“H” : ON, “L” : OFF) (Not used.)
3	LMUT2	O	L-ch, “0” detection output. (“H” : ON, “L” : OFF) (Not used.)
4	CKOUT	O	Master clock frequency division output (Not used.)
5	VDD0	—	Digital power supply
6	SBSO	O	Serial output of sub-P to W.
7	EXCK	I	Clock input for SBSO read output.
8	SQCK	I	Clock input for SQSO read output.
9	SQSO	O	SubQ 80 bit, PCM peak and level data 16 bit output.
10	SENS	O	SENS output. Output to CPU.
11	SCLK	I	Clock input for SENS real data read.
12	DATA	I	Serial data input from CPU.
13	XLAT	I	Latch input from CPU. Latch serial data at the falling edge.
14	CLOK	I	Serial data transfer clock input from CPU.
15	XRST	I	System reset (“L” : Reset)
16	ACDT	O	Not used.
17	PWM1	I	External control input of spindle motor.
18	XLON	O	Microcomputer extension interface (Output) (Not used.)
19	SPOA	I	Microcomputer extension interface (Input A) (Not used.)
20	WFCK	O	WFCK (Write Flame Clock) output
21	GTOP	O	GTOP output
22	XUGF	O	XUGF output (Not used.)
23	XPCK	O	XPLCK output (Not used.)
24	GFS	O	GFS output
25	RFCK	O	RFCK output
26	C2PO	O	C2PO output (Not used.)
27	XROF	O	XROF output
28	SCOR	O	“H” output at either detection, sub code sync S0 or S1.
29	MNT0	O	MNT0 output (Not used.)
30	MNT1	O	MNT1 output (Not used.)
31	MNT3	O	MNT3 output (Not used.)
32	VSS1	—	Digital GND
33	DOUT	O	Digital-Out output
34	ATSK	I	For anti-shock.
35	MIRR	O	Mirror signal output (Not used.)
36	DFCT	O	Diffect signal output (Not used.)
37	FOK	O	Focus OK signal output
38	VDD1	—	Digital power supply
39	VPCO1	O	Charge pump output for wideband EFM PLL.
40	VPCO2	O	VCO2 charge pump output for wideband EFM PLL.
41	VCK.I	I	VCO2 oscillator input for wideband EFM PLL.
42	V16M	O	VCO2 oscillator output for wideband EFM PLL.
43	VCTL	I	VCO2 control input for wideband EFM PLL.
44	PCO	O	Charge pump output for master PLL.
45	FILO	O	Filter output for master PLL (Slave = digital PLL).
46	FILI	I	Filter input for master PLL.
47	AVSS4	—	Analog GND
48	CLTV	I	VCO control voltage input for master.
49	AVDD4	—	Analog power supply
50	RFAC	I	EFM signal input
51	BIAS	I	Asymmetry circuit constant current input
52	ASY.I	I	Asymmetry comparate voltage input

Pin No.	Pin Name	I/O	Pin Description
53	ASY.O	O	EFM full-swing output (“L” : VSS, “H” : VDD)
54	VC	I	Center voltage input
55	FE	I	Focus error signal input
56	SE	I	Sled error signal input
57	TE	I	Tracking error signal input
58	CE	I	Center error signal input
59	RFDC	I	RF signal input
60	RFC	I	Condenser connection pin for LPF time constant of RF signal.
61	ADIO	O	OP amplifier output (Not used.)
62	AVSS3	—	Analog GND
63	IGEN	I	Current source reference resistor connection for OP amplifier.
64	AVDD3	—	Analog power supply
65, 66	TES2, 3	I	TEST pin (Fixed at “L”.)
67	VSS2	—	Digital GND
68	TEST	I	TEST pin (Fixed at “L”.)
69	SFDR	O	Sled drive output
70	SRDR	O	Sled drive output
71	TFDR	O	Tracking drive output
72	TRDR	O	Tracking drive output
73	FFDR	O	Focus drive output
74	FRDR	O	Focus drive output
75	VDD2	—	Digital power supply
76	COUT	O	Track number count signal output (Not used.)
77	LOCK	O	Not used.
78	MDS	O	Servo control output of spindle motor. (Not used.)
79	MDP	O	Servo control output of spindle motor.
80	SSTP	I	Disc most inner track detection signal input
81	FSTO	O	2/3 frequency division output of pins 103 and 104.
82	FSTI	I	Reference clock input for digital servo.
83	XTSL	I	X’tal select input (“L” : 16.9344 MHz)
84	C4M	O	4.2336 MHz output
85	WDCK	O	D/A interface. Word clock f = 2Fs
86	VDD3	—	Digital power supply
87	LRCK	O	D/A interface. LR clock f = Fs
88	LRCKI	I	LR clock input to DAC. (48 bit slot) (Not used.)
89	PCMD	O	D/A interface. Serial data (2’s COMP, MSB first)
90	PCMDI	I	Audio data input to DAC. (48 bit slot) (Not used.)
91	BCK	O	D/A interface. Bit clock
92	BCKI	I	Bit clock input to DAC. (48 bit slot) (Not used.)
93	EMPH	O	Not used.
94	EMPHI	I	De-emphasis ON/OFF of DAC. (“H” : ON, “L” : OFF) (Not used.)
95	VSS3	—	Digital GND
96	AVSS1	—	L-ch, Analog GND.
97	AVDD1	—	L-ch, Analog power supply.
98	AOUT1	O	L-ch, Analog output. (Not used.)
99	AIN1	I	L-ch, OP amplifier input. (Not used.)
100	LOUT1	O	L-ch, LINE output. (Not used.)
101	AVSS1	—	L-ch, Analog GND.
102	XVDD	—	Analog power supply for master clock.
103	XTAI	I	X’tal oscillator input of master clock (16.9344 MHz).
104	XTAO	O	X’tal oscillator output of master clock. (Not used.)
105	XVSS	—	Analog GND for master clock.
106	AVSS2	—	R-ch, Analog GND.

Pin No.	Pin Name	I/O	Pin Description
107	ROUT2	O	R-ch, LINE output. (Not used.)
108	AIN2	I	R-ch, OP amplifier input. (Not used.)
109	AOUT2	O	R-ch, Analog output. (Not used.)
110	AVDD2	—	R-ch, Analog power supply.
111	AVSS2	—	R-ch, Analog GND.
112	VSS0	—	Digital GND

• IC300 MB90F574PFV-G-140-BND (SYSTEM CONTROL)

Pin No.	Pin Name	I/O	Pin Description
1	TIR WR	O	TIR IC data write output
2	TIR RD	O	TIR IC data read output
3	TIR CE	O	TIR IC data chip enable output
4	$\overline{\text{TIR CE}}$	O	XTIR IC data chip enable output
5	TIR BUSY	I	TIR IC busy input
6	TIR PDOWN	O	TIR IC power down output
7	DIVER	O	FM diversity ON/OFF output (Not used in this set.)
8	VCC	—	Power supply pin (+5 V)
9	AF SEEK	O	AF SEEK output
10	WIDE	O	WIDE/NARROW select output
11	CAUTION	I	Caution alarm setting (Fixed at “H” in this set.)
12	$\overline{\text{NOSE SW}}$	I	Nose detection input
13	COLOR	O	Color control output (“H”:green, “L”:amber)
14	$\overline{\text{BUSON}}$	O	Bus ON control output
15	BEEP	O	BEEP output
16	TIR RES	O	TIR IC reset (Power down) output
17	DF LAT	O	Digital filter latch output
18	DF SO	O	Digital filter serial data output
19	DF CKO	O	Digital filter clock output
20	UNISI	I	Serial data input (for SONY BUS)
21	UNISO	O	Serial data output (for SONY BUS)
22	UNICK	O	Serial clock output (for SONY BUS)
23	NCO	—	Not used.
24	SIRCS	I	Remote commander input
25	PLLSI	I	PLL data input
26	PLLSO	O	PLL data output
27	PLLCKO	O	PLL clock output
28	PLL CE	O	PLL chip enable output
29	P MOT+	O	Front panel motor control (+) output
30	P MOT–	O	Front panel motor control (–) output
31	I DET	I	Panel motor lock detection input
32	POS0	I	Position detection input 0 (Open end)
33	GND	—	GND
34	C	—	Power stabilization capacitor pin
35	POS1	I	Position detection input 1 (Close end)
36	POS2	I	Position detection input 2 (10 DEG.)
37	POS3	I	Position detection input 3 (20 DEG.)
38	DVCC	—	D/A converter VREF input
39	DVSS	—	GND of D/A converter.
40	MOTREF	O	Motor reference voltage output
41	LCDANG	O	LCD view angle adjustment analog output
42	AVCC	—	Analog power supply pin (+5 V)
43	AVRH	—	A/D converter VREF+ input
44	AVRL	—	A/D converter VREF– input
45	AVSS	—	Analog GND
46	DSTSEL0	I	Destination select input 0 (Fixed at “H” in this set.)
47	H TEMP	I	High templature detection analog input (Fixed at “H” in this set.)
48	L TEMP	I	Low templature detection analog input (Fixed at “H” in this set.)
49	MPT	I	Tuner multi-pass input
50	VSM	I	S-Meter voltage detection input
51	RC IN0	I	Rotary commander input 0
52, 53	KEYIN0, 1	I	Key input 0, 1

Pin No.	Pin Name	I/O	Pin Description
54	VCC	—	Power supply pin (+5 V)
55	RAMBU	I	RAM reset detection input
56	$\overline{\text{TESTIN}}$	I	Test mode setting detection input
57	$\overline{\text{AD ON}}$	O	Power control output of A/D conversion.
58, 59	RE IN0, 1	I	Rotary encoder input 0, 1
60	$\overline{\text{BOOT}}$	I	Compulsory boot mode input
61	DIMMER	O	Dimmer control output
62	TIR IND	O	TIR indicator control output
63	GND	—	GND
64	$\overline{\text{SYSRST}}$	O	System reset output
65, 66	NCO	—	Not used.
67	EEDATA	I/O	EEPROM serial data input/output
68	EECLK	O	EEPROM serial clock output
69	NCO	—	Not used.
70	RDSSI	I	RDS serial clock input
71	RDSCKO	I	RDS serial data input
72	DAVN	I	RDS IC data taking in detection input
73	X0A	—	Low speed oscillation input (32.768 kHz)
74	X0B	—	Low speed oscillation input (32.768 kHz)
75	RC IN1	I	Rotary commander input
76	BU IN	I	Back-up power detection input
77	KEY ACK	I	Key input acknowledge
78	$\overline{\text{ILLIN}}$	I	Illumination line detection input
79	TEL ATT	I	Telephone mute detection input
80	NCO	—	Not used.
81	$\overline{\text{ACC IN}}$	I	Accessory power detection input
82	EMPH I	I	Emphasis input
83	FP CLOSE	I	Front panel close detection input
84	FP OPEN	O	Front panel open control output
85	BOOT DP	O	Display controller boot mode control output
86	HSTX	—	Connect to power supply pin.
87	MD2	—	Connect to GND.
88, 89	MD0, 1	—	Connect to power supply pin.
90	$\overline{\text{RESET}}$	I	Microcomputer reset input
91	VSS	—	GND
92	X0	—	High speed oscillation input (3.68 MHz)
93	X1	—	High speed oscillation input (3.68 MHz)
94	VCC	—	Power supply pin (+5 V)
95	TIMPOL	O	Time poling setting (Fixed at “H” in this set.)
96	PW ON	O	System power control output
97	ILL ON	O	Illumination power control output
98	DIRECT	O	Direct volume control output
99	ATT	O	System mute control output
100	ANTREM	O	Antenna remote control output
101	VOLCE0	O	Input selector/tone/sub volume serial chip enable output
102	VOLCE1	O	Electric volume serial chip enable output (L-CH)
103	VOLCE2	O	Electric volume serial chip enable output (R-CH)
104	VOLCKO	O	Volume serial clock output
105	VOLSO	O	Volume serial data output
106	ENC+	I	Rotary commander and encoder input (+)
107	ENC–	I	Rotary commander and encoder input (–)
108	FM ON	O	FM ON control output
109	AM ON	O	AM ON control output

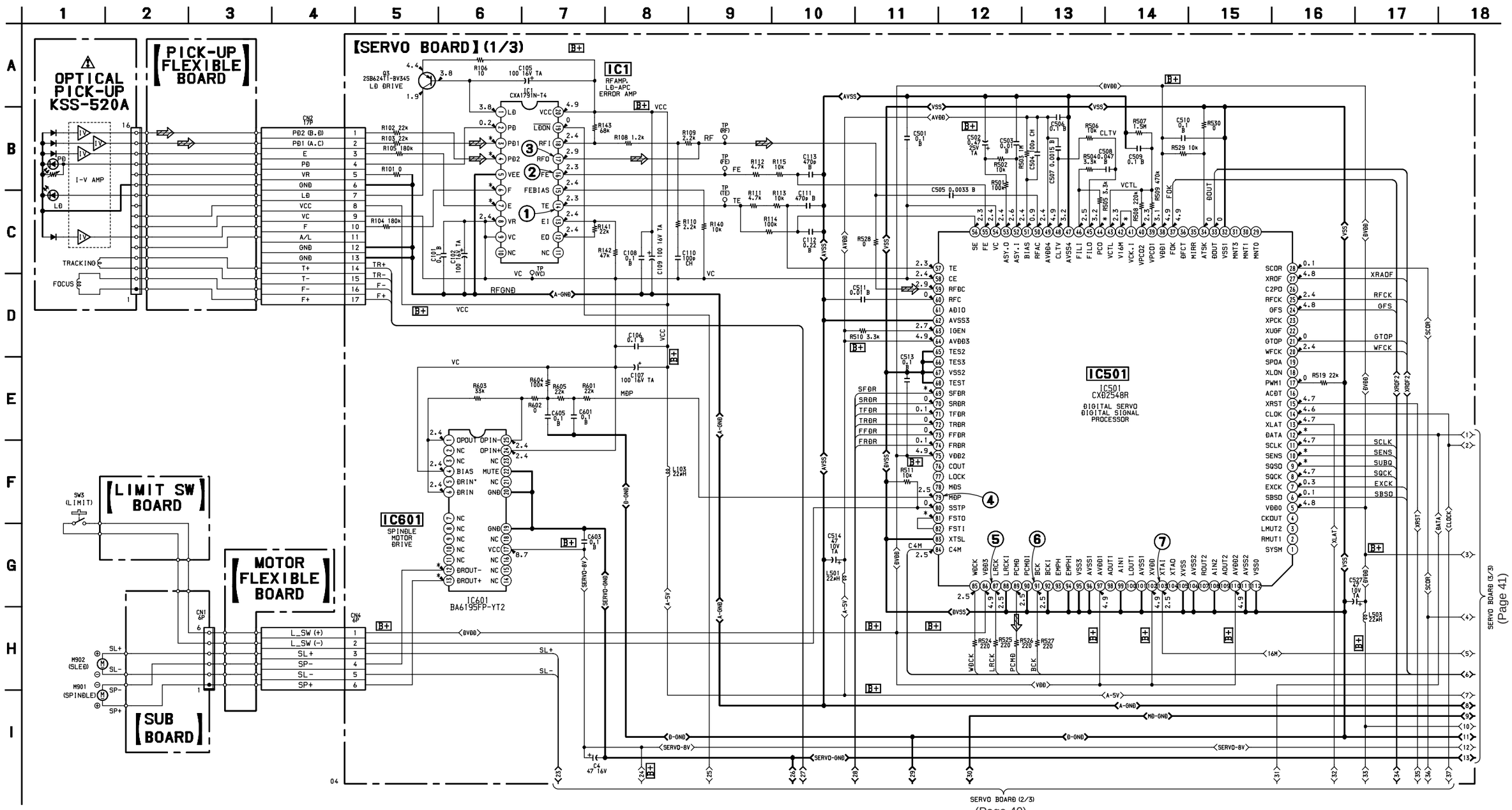
Pin No.	Pin Name	I/O	Pin Description
110	SEEKOUT	O	SEEK OUT output
111	AM STIN	I	AM stereo input (Not used in this set.)
112	FM STIN	I/O	Used in conjunction with stereo input/monaural output (FM mode)
113	SD IN	I	Signal detector input
114	TU ATT	O	Tuner mute output
115	TIR D0	I/O	TIR IC data 0 input/output
116	TIR D1	I/O	TIR IC data 1 input/output
117	TIR D2	I/O	TIR IC data 2 input/output
118	TIR D3	I/O	TIR IC data 3 input/output
119	VSS	—	GND
120	TIRPLAY	O	TIR IC play mode audio select control output

• IC500 HD6413002F16 (DISPLAY CONTROL)

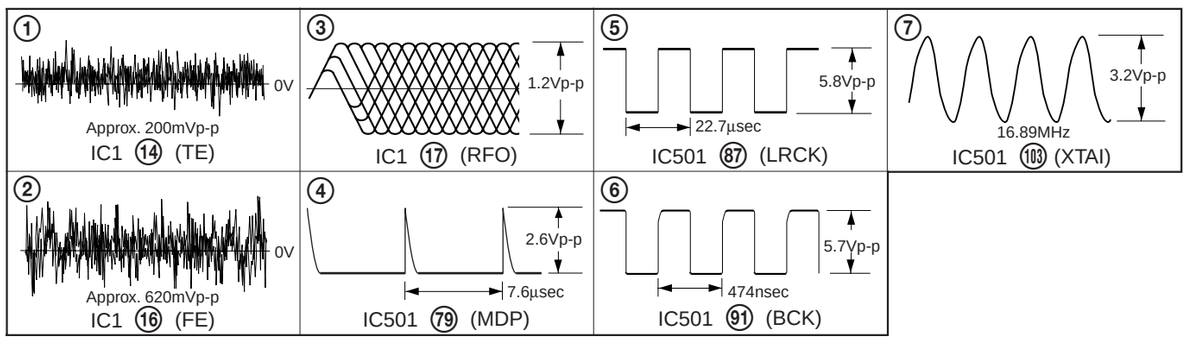
Pin No.	Pin Name	I/O	Pin Description
1	VDD	—	Power supply pin (+5 V)
2	SIRCS	I	Remote commander input
3	SIRCS	I	Remote commander input
4	$\overline{\text{LCD-RST}}$	O	LCD controller reset control output
5	ILL ON	O	LCD controller power supply control output
6	EL ON	O	LCD back light EL power supply control output
7	LCD-ST	O	LCD controller information start request signal output
8	CS-CTL	O	SRAM master chip enable control output (Not used in this set.)
9	BOOTI	I	Compulsory boot mode input
10	(RESO)	O	Connect to GND.
11	VSS	O	GND
12	LCD-SO	O	LCD controller serial data output
13	UNI-SO	O	BUS interface data output
14	LCD-RX	I	LCD controller serial data input
15	UNI-SI	I	BUS interface data input
16	UNI-CO	O	LCD controller serial clock ouput
17	UNI-CI	I	LCD controller serial clock input
18 – 21	D0 – D3	I/O	External RAM, ROM data bus input/output
22	VSS	—	GND
23 – 34	D4 – D15	I/O	External RAM, ROM data bus input/output
35	VDD	—	Power supply pin (+5 V)
36 – 43	A0 – A7	O	External RAM, ROM address bus output
44	VSS	—	GND
45 – 56	A8 – A19	O	External RAM, ROM address bus output
57	VSS	—	GND
58	$\overline{\text{WAIT}}$	O	Not used.
59	(P61)	—	Not used.
60	(P62)	—	Not used.
61	NC	—	Not used.
62	$\overline{\text{STBY}}$	I	Hardware standby input (Fixed at “H”.)
63	$\overline{\text{SYSRST}}$	I	Reset input
64	BU-IN	I	Back-up power detection input
65	VSS	—	GND
66	EXTAL	O	Oscillation output (14.74 MHz)
67	XTAL	I	Oscillation input (14.74 MHz)
68	VDD	—	Power supply pin (+5 V)
69	$\overline{\text{AS}}$	—	Not used.
70	$\overline{\text{RD}}$	O	Read signal output
71	$\overline{\text{HWR}}$	O	High write signal output
72	$\overline{\text{LWR}}$	O	Low write signal output
73	MD0	I	Microcomputer operation mode input (Fixed at “L”.)
74	MD1	I	Microcomputer operation mode input (Fixed at “L”.)
75	MD2	I	Microcomputer operation mode input (Fixed at “H”.)
76	AVDD	I	A/D converter power supply input
77	VREF	I	A/D converter reference voltage input
78 – 83	(AN0 – AN5)	—	Connect to GND.
84	BU-IN	I	Back-up power detection input
85	PBS	I	Parking brake input
86	AVSS	—	A/D converter GND
87	$\overline{\text{BUS-ON}}$	I	BUS-interface BUS-ON input
88	$\overline{\text{SRAM-CS}}$	O	SRAM chip enable output
89	$\overline{\text{DEC-CS}}$	O	Demodulator LSI chip enable output (Not used in this set.)

Pin No.	Pin Name	I/O	Pin Description
90	$\overline{\text{DEC-INT}}$	O	Demodulator LSI initial output (Not used in this set.)
91	$\overline{\text{ROM-CS}}$	O	PROM chip enable output
92	VSS	—	GND
93	UNI-REQ	O	Not used.
94	LINK-OFF	O	BUS interface link output
95	DEC-ON	O	Not used.
96	$\overline{\text{DEC-CLR}}$	O	Demodulator LSI reset output (Not used in this set.)
97 – 99	A21 – A23	O	Not used.
100	A20	O	External RAM, ROM address bus output

3-7. SCHEMATIC DIAGRAM — CD MECHANISM SECTION (1/3) — • Refer to page 63 for IC Block Diagrams.



• **Waveforms** (MODE:PLAY)



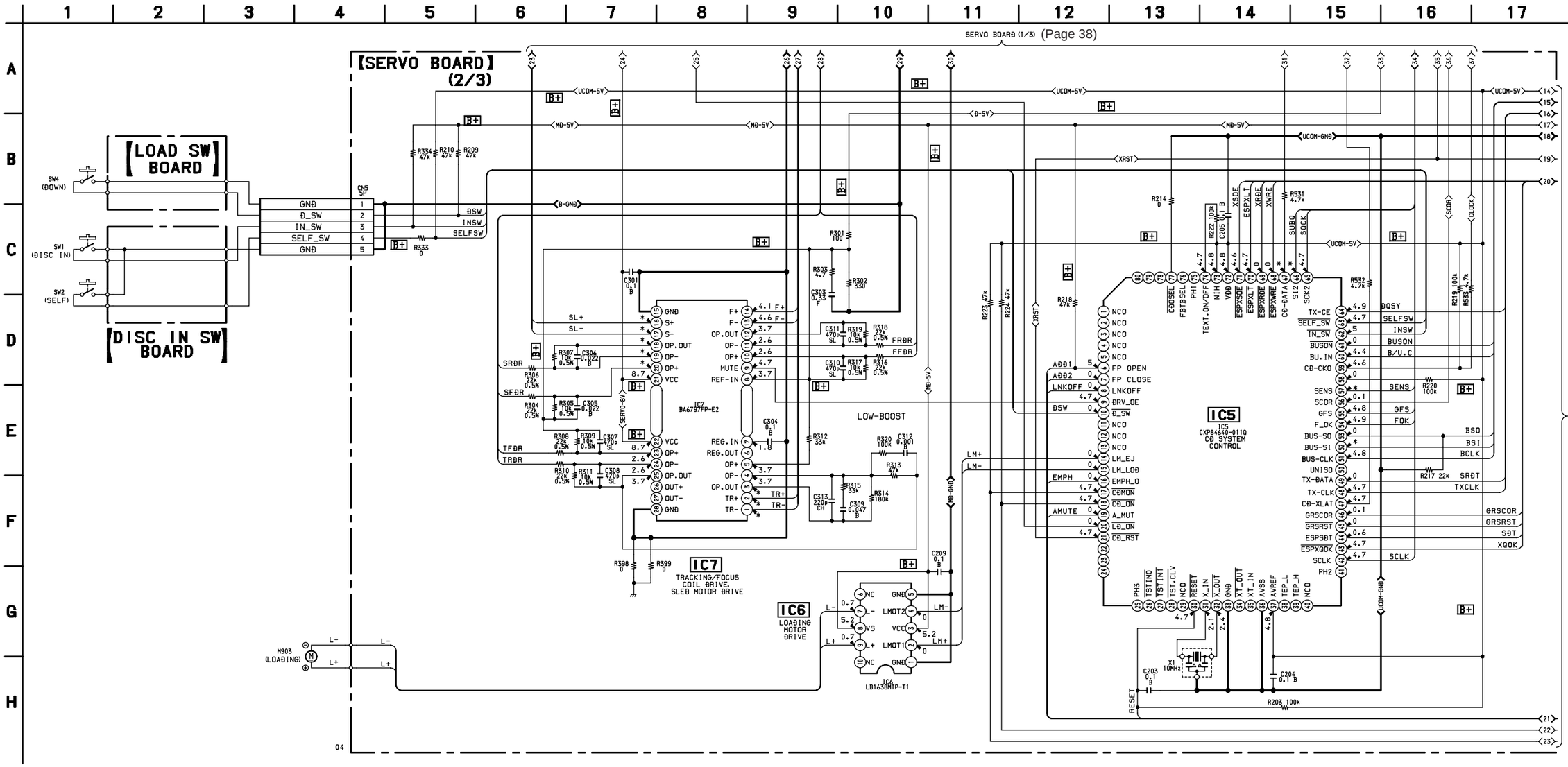
Note:
- All capacitors are in µF unless otherwise noted. pF: µµF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- % : indicates tolerance.

Note: The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

- B+ : B+ Line.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.

- Voltage and waveforms are dc with respect to ground under no-signal conditions.
  no mark : CD PLAY
  ∗ : Impossible to measure
- Voltages are taken with a VOM (Input impedance 10 MΩ). Voltage variations may be noted due to normal production tolerances.
- Waveforms are taken with a oscilloscope. Voltage variations may be noted due to normal production tolerances.
- Signal path.
  ⇨ : CD

3-8. SCHEMATIC DIAGRAM — CD MECHANISM SECTION (2/3) — • Refer to page 63 for IC Block Diagrams.



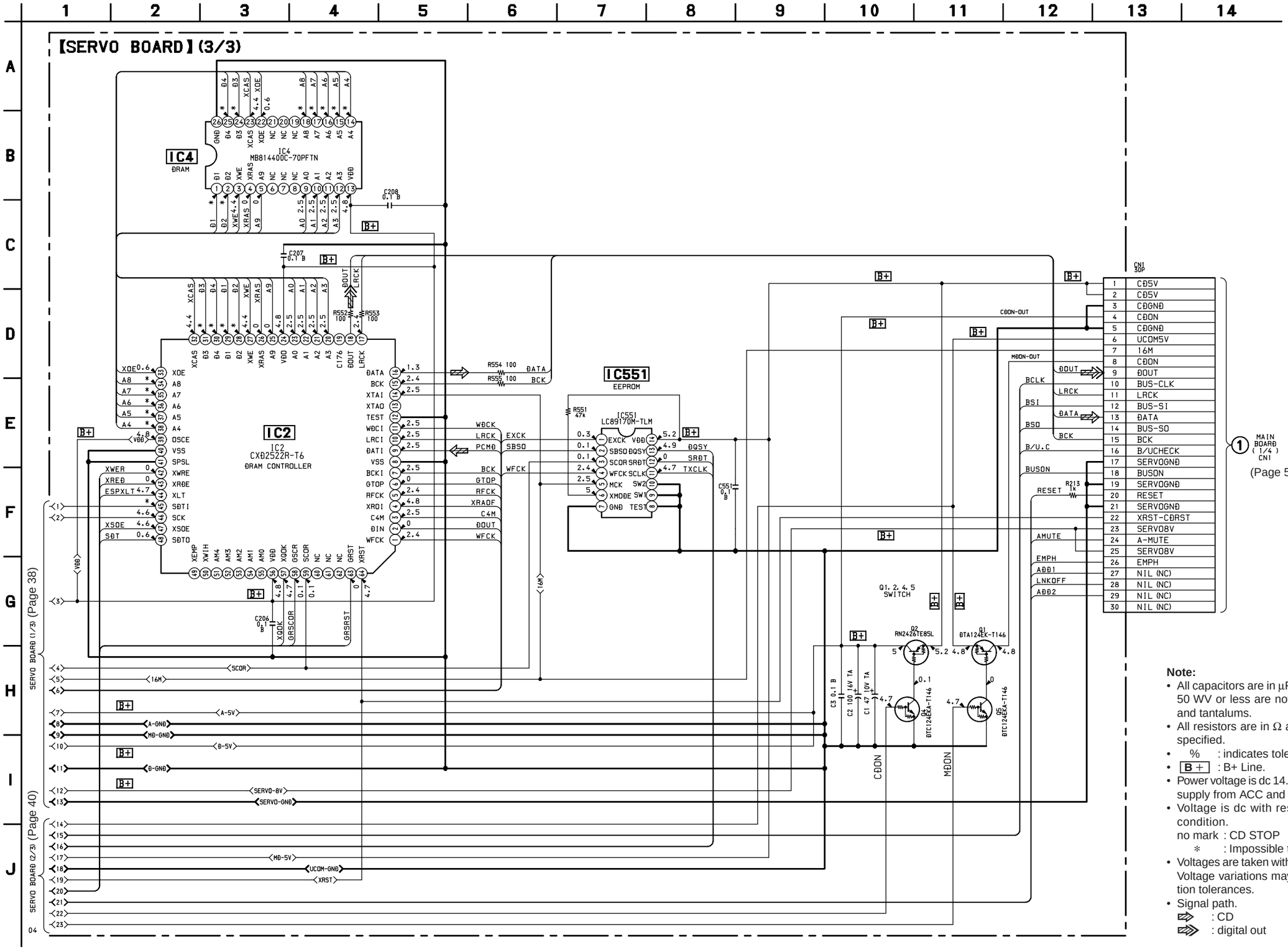
Note:

- All capacitors are in μF unless otherwise noted. pF: μμF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- % : indicates tolerance.
- △ : internal component.

Note: The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

- B + : B+ Line.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.
- Voltage is dc with respect to ground under no-signal condition.
  no mark : CD PLAY
  ✻ : Impossible to measure
- Voltages are taken with a VOM (Input impedance 10 MΩ). Voltage variations may be noted due to normal production tolerances.

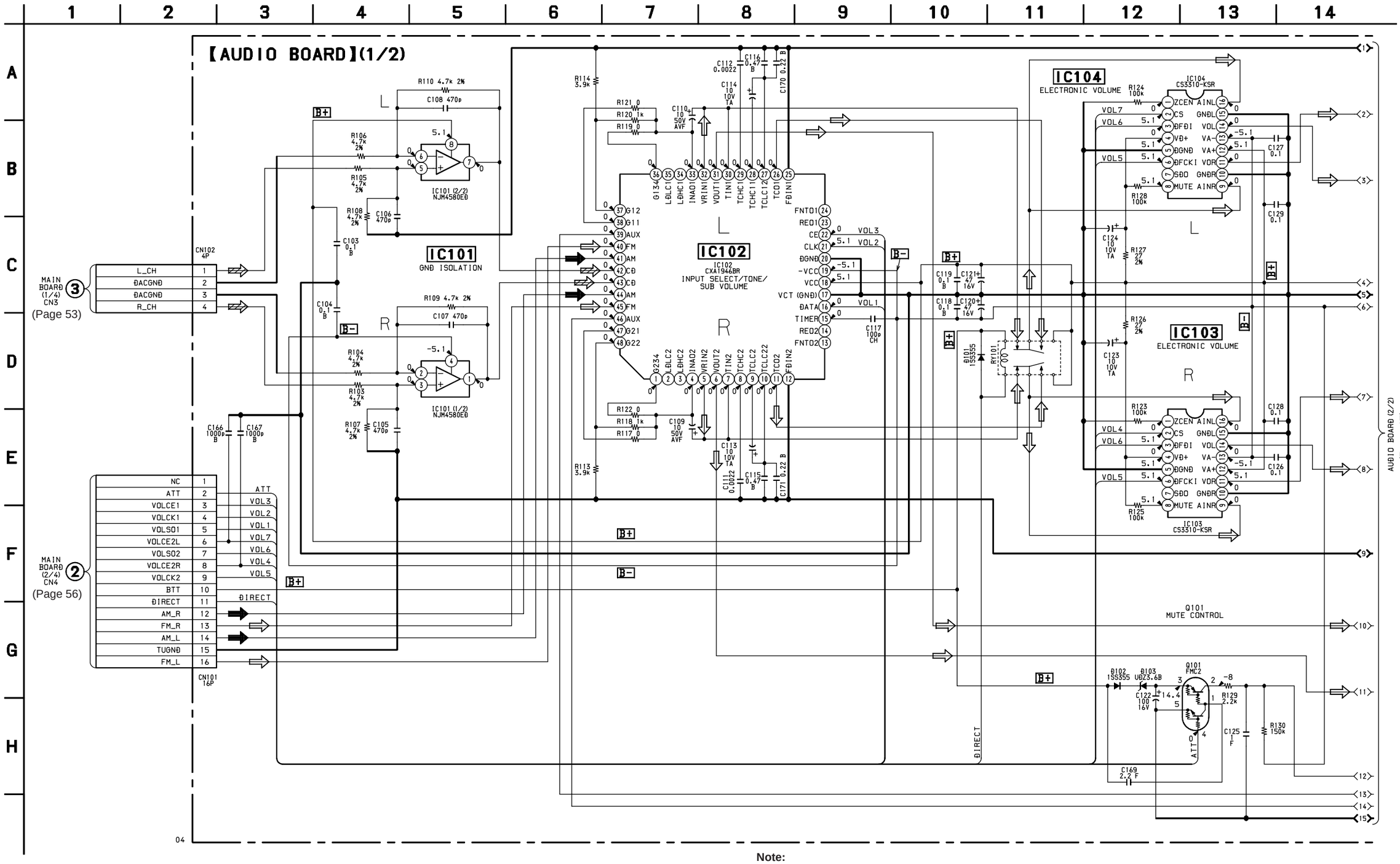
3-9. SCHEMATIC DIAGRAM — CD MECHANISM SECTION (3/3) — • Refer to page 63 for IC Block Diagrams.



Note:

- All capacitors are in μF unless otherwise noted. pF: μμF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- % : indicates tolerance.
- B+ : B+ Line.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.
- Voltage is dc with respect to ground under no-signal condition.
  no mark : CD STOP
  * : Impossible to measure
- Voltages are taken with a VOM (Input impedance 10 MΩ). Voltage variations may be noted due to normal production tolerances.
- Signal path.
  : CD
  : digital out

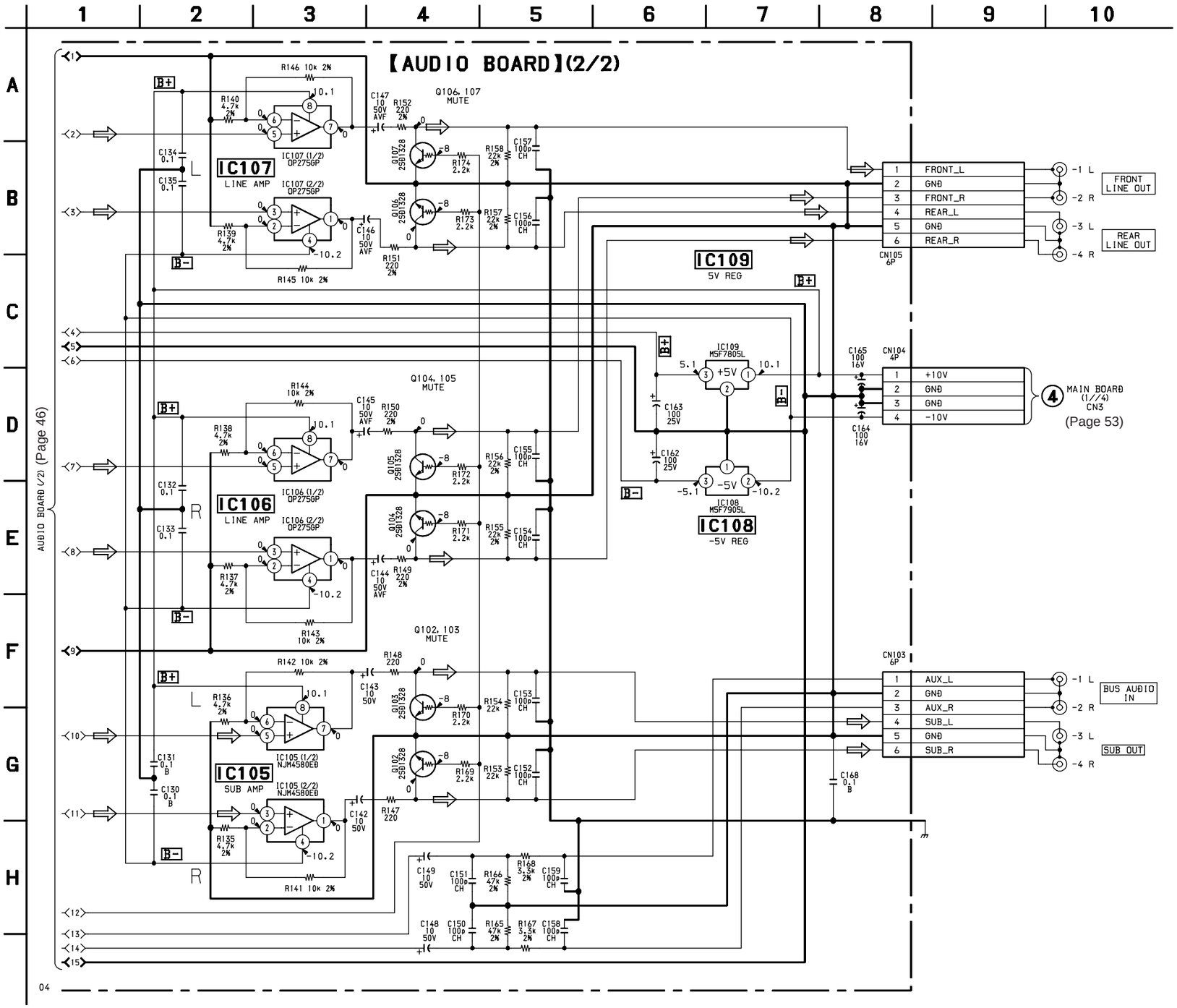
3-11. SCHEMATIC DIAGRAM — AUDIO SECTION (1/2) — • Refer to page 65 for IC Block Diagrams.



Note:

- All capacitors are in µF unless otherwise noted. pF: µµF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- % : indicates tolerance.
- B+ : B+ Line.
- B– : B– Line.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.
- Voltage is dc with respect to ground under no-signal (detuned) condition.
  no mark : FM
  * : Impossible to measure
- Voltages are taken with a VOM (Input impedance 10 MΩ). Voltage variations may be noted due to normal production tolerances.
- Signal path.
  : FM
  : MW
  : CD

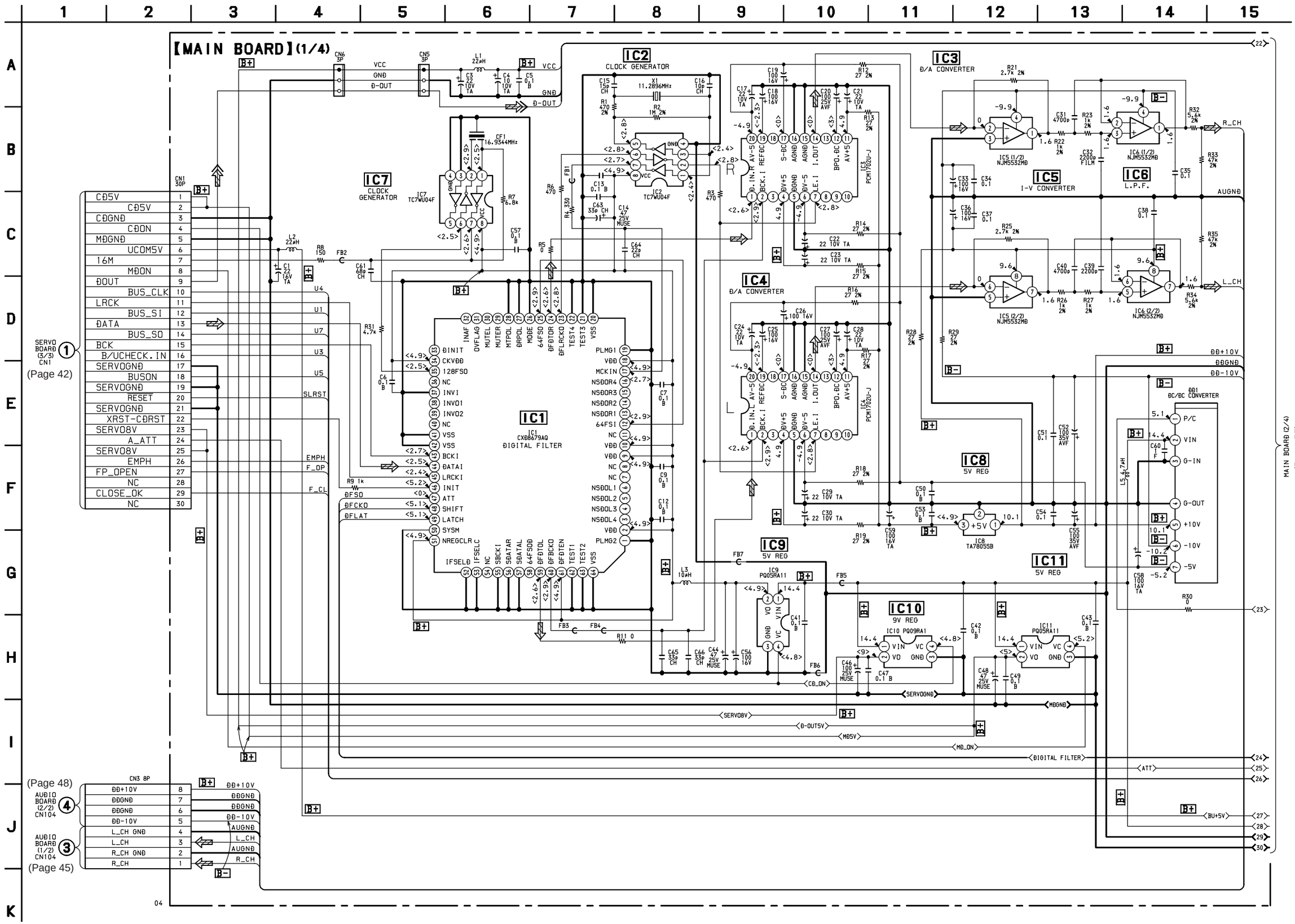
3-12. SCHEMATIC DIAGRAM — AUDIO SECTION (2/2) —



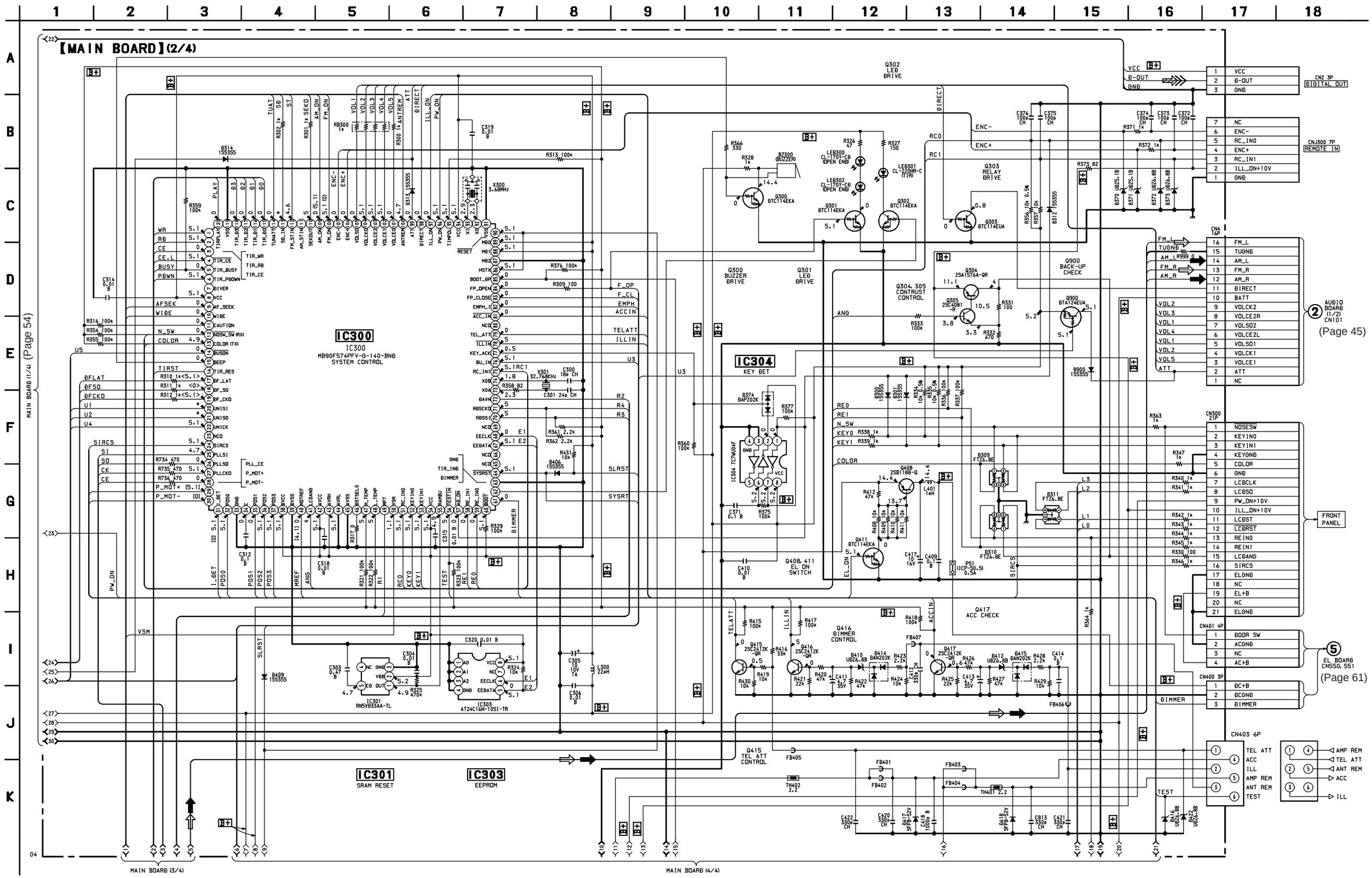
Note:

- All capacitors are in μF unless otherwise noted. pF: μμF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- % : indicates tolerance.
- △ : internal component.
- ▭ : panel designation.
- B+ : B+ Line.
- ▬ : adjustment for repair.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.
- Voltage is dc with respect to ground under no-signal (detuned) condition.
  no mark : FM
  ( ) : MW
  < > : CD PLAY
  [ ] : PANEL MOTOR operation
  * : Impossible to measure
- Voltages are taken with a VOM (Input impedance 10 MΩ). Voltage variations may be noted due to normal production tolerances.
- Signal path.
  ⇨ : FM
  ➡ : MW
  ⇨ : CD
  ⇨ : digital out
- Abbreviation
  G : German model.

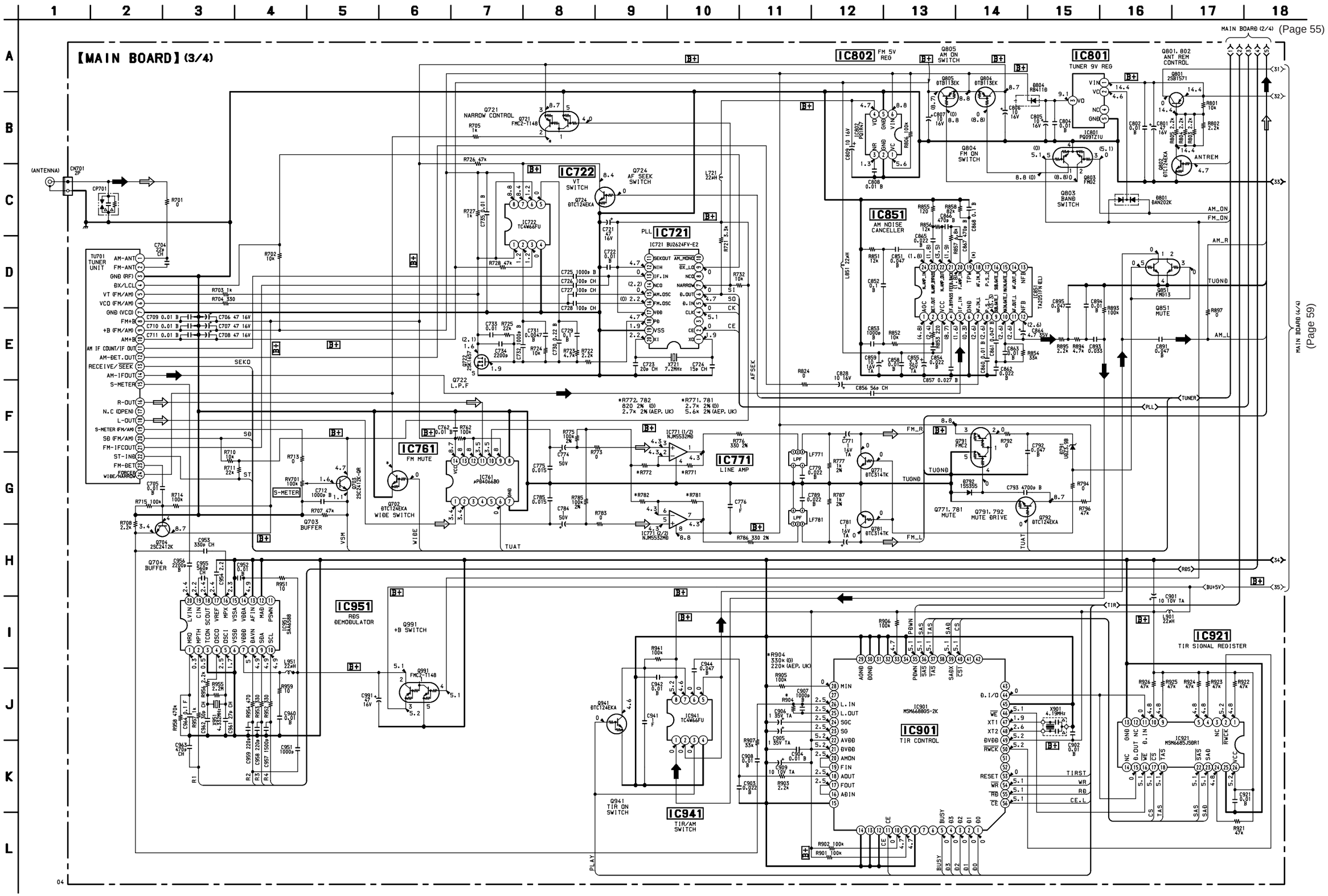
3-14. SCHEMATIC DIAGRAM — MAIN SECTION (1/4) — • Refer to page 48 for Note and Refer to page 63 for IC Block Diagrams.



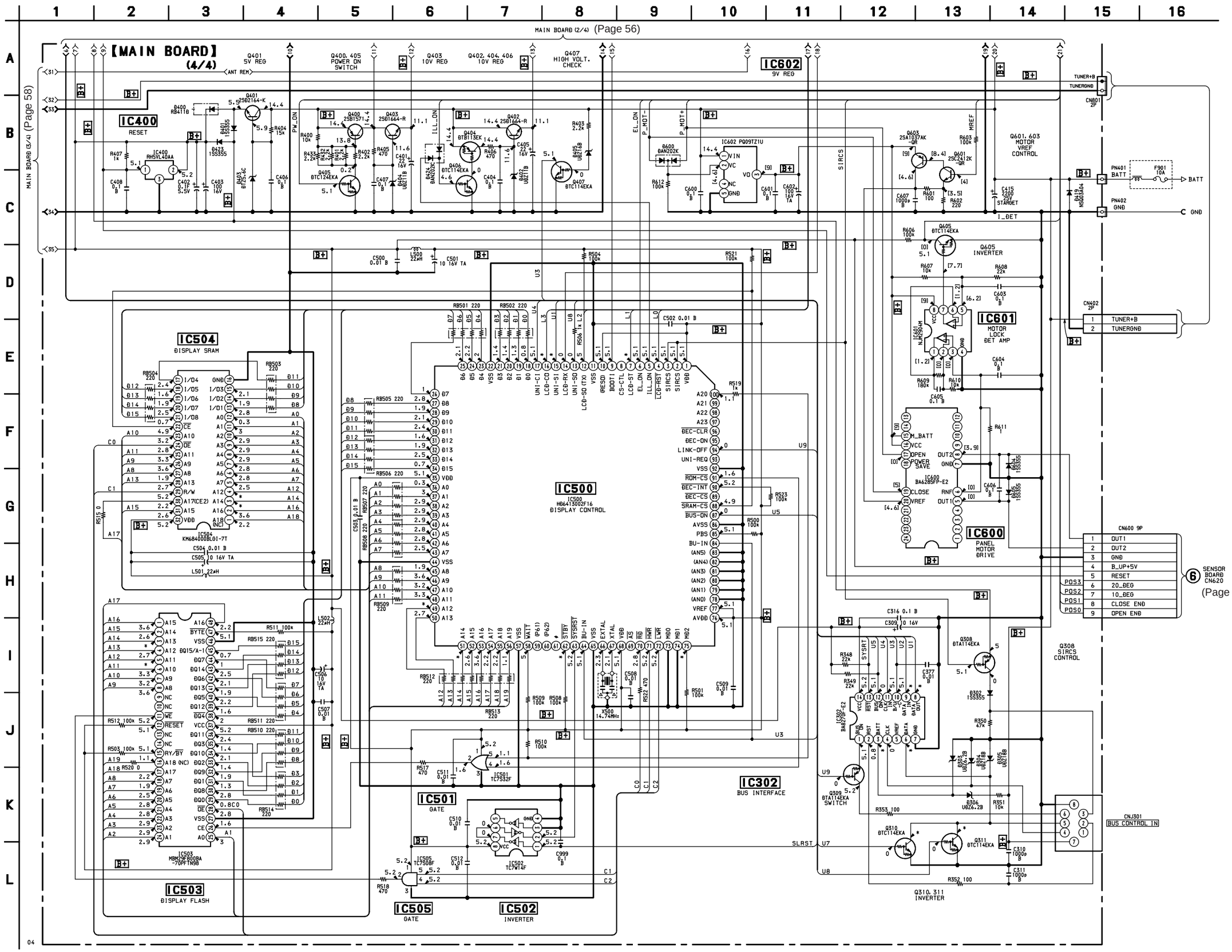
3-15. SCHEMATIC DIAGRAM — MAIN SECTION (2/4) — • Refer to page 48 for Note and Refer to page 66 for IC Block Diagrams.



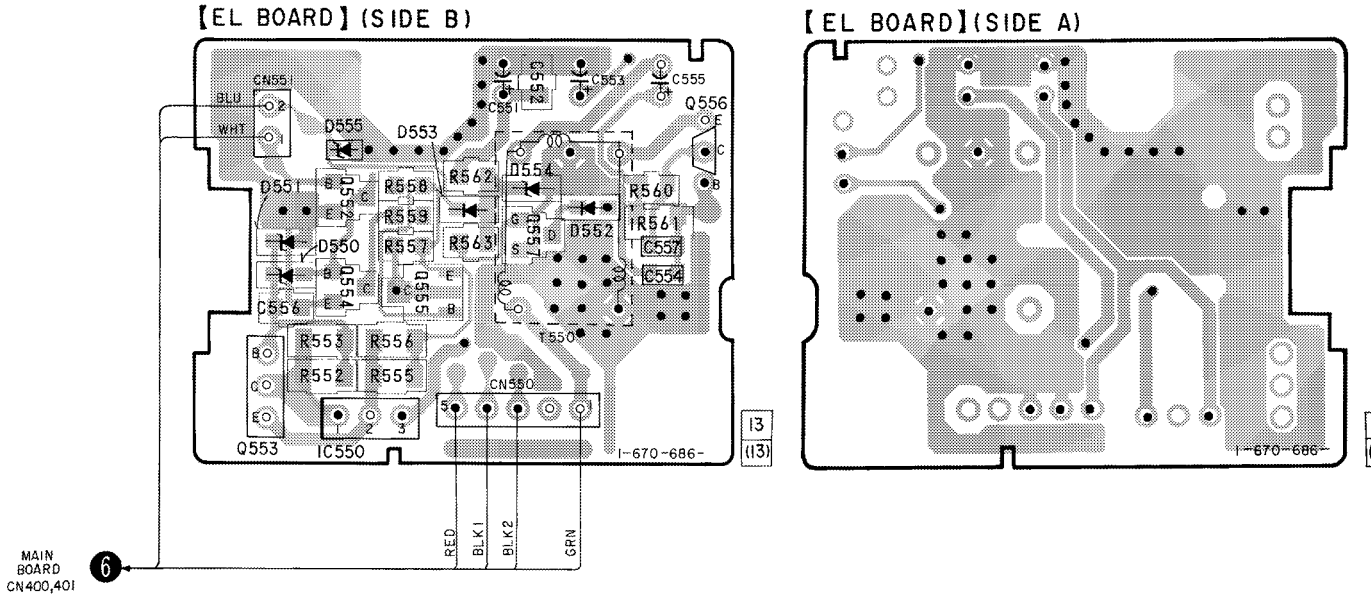
3-16. SCHEMATIC DIAGRAM — MAIN SECTION (3/4) — • Refer to page 48 for Note and Refer to page 67 for IC Block Diagrams.



3-17. SCHEMATIC DIAGRAM — MAIN SECTION (4/4) — • Refer to page 48 for Note and Refer to page 66 for IC Block Diagrams.



3-18. PRINTED WIRING BOARD — EL SECTION —

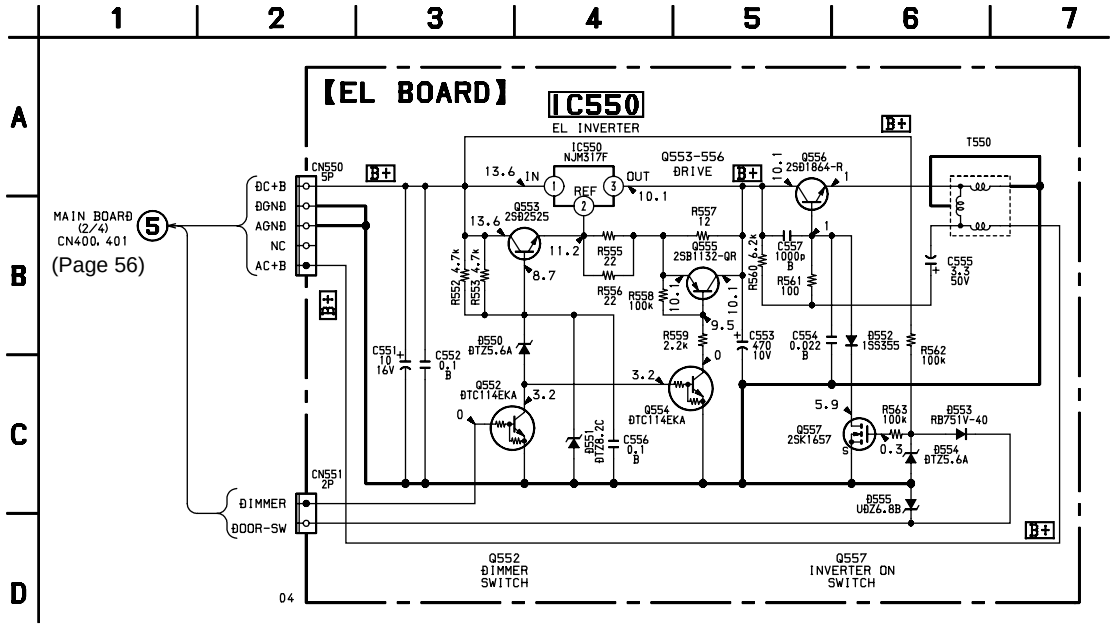


(Page 52)

Note:
- ○——— : parts extracted from the component side.
- ● : Through hole.
- ▒▒▒ : Pattern from the side which enables seeing. (The other layer's patterns are not indicated.)

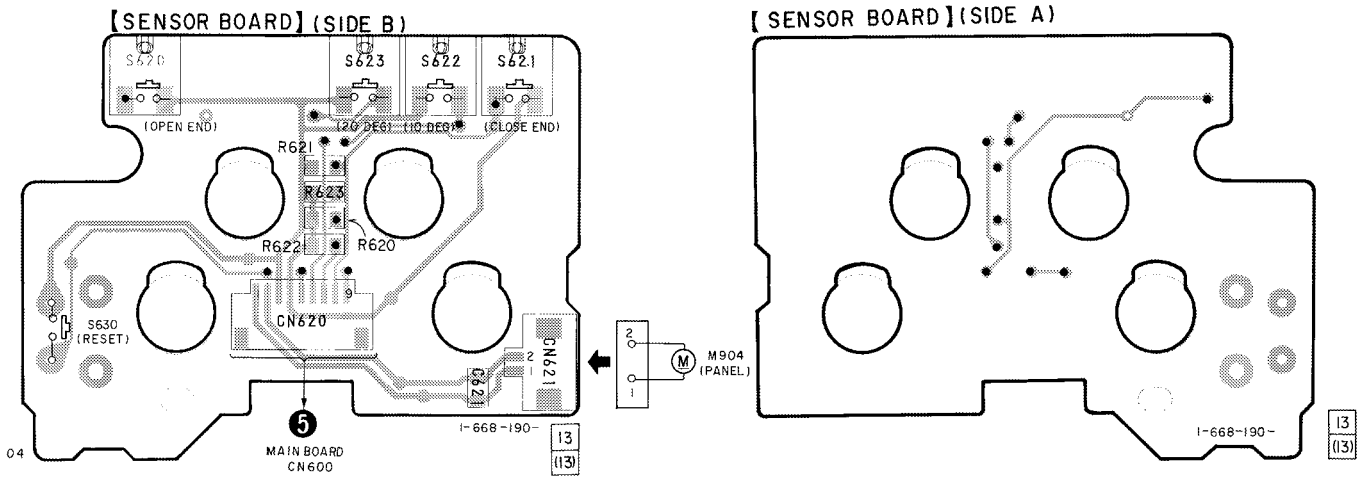
Caution:	
Pattern face side: (Side B)	Parts on the pattern face side seen from the pattern face are indicated.
Parts face side: (Side A)	Parts on the parts face side seen from the parts face are indicated.

3-19. SCHEMATIC DIAGRAM — EL SECTION —



Note:
- All capacitors are in µF unless otherwise noted. pF: µµF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- B+ : B+ Line.
- Power voltage is dc 14.4V and fed with regulated dc power supply from ACC and BATT cords.
- Voltage is dc with respect to ground under no-signal (detuned) condition.
  no mark : FM

3-20. PRINTED WIRING BOARD — SENSOR SECTION —



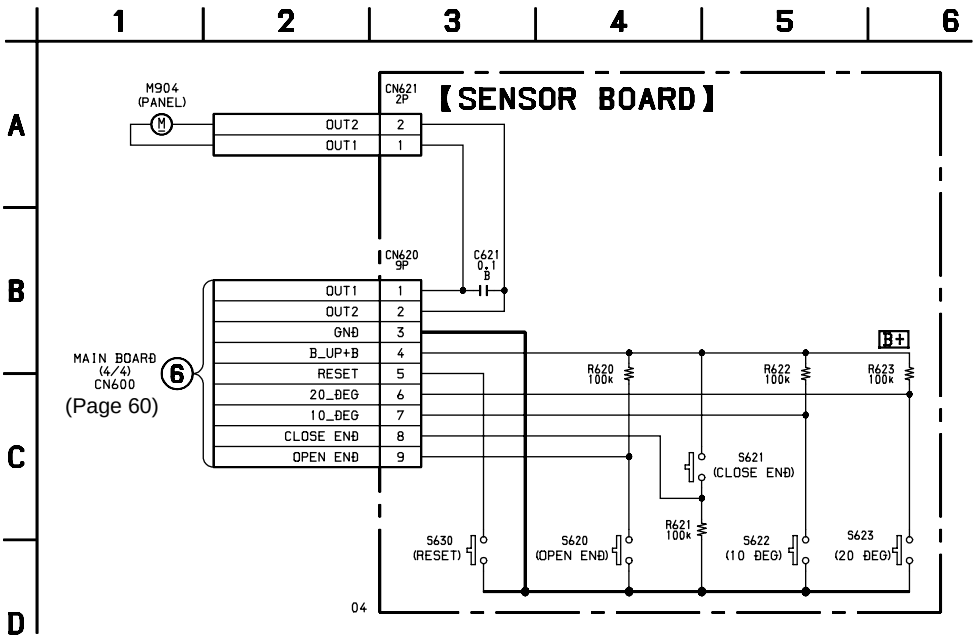
(Page 49)

Note:

- ○——— : parts extracted from the component side.
- ● : Through hole.
- ▒▒▒ : Pattern from the side which enables seeing. (The other layer's patterns are not indicated.)

Caution:	
Pattern face side: (Side B)	Parts on the pattern face side seen from the pattern face are indicated.
Parts face side: (Side A)	Parts on the parts face side seen from the parts face are indicated.

3-21. SCHEMATIC DIAGRAM — SENSOR SECTION —

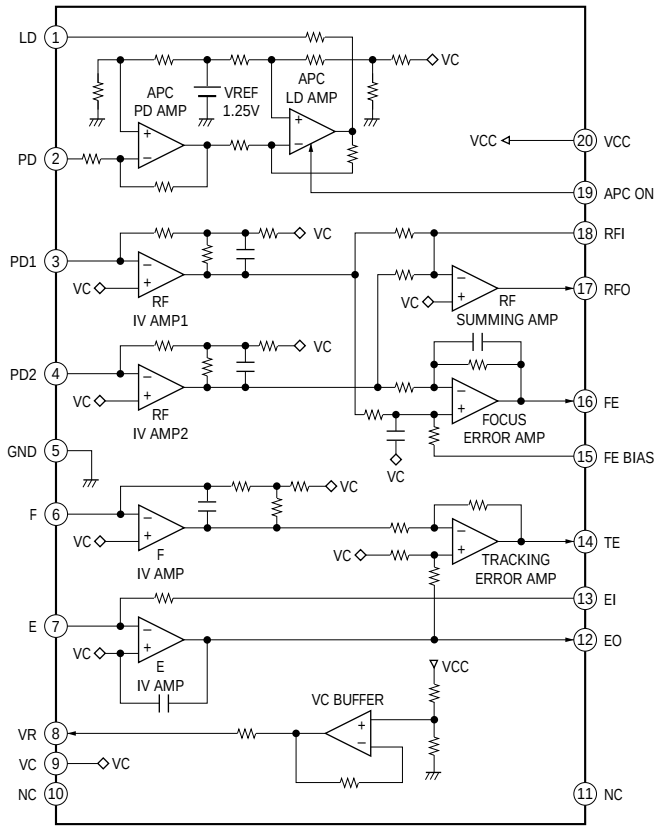


Note:

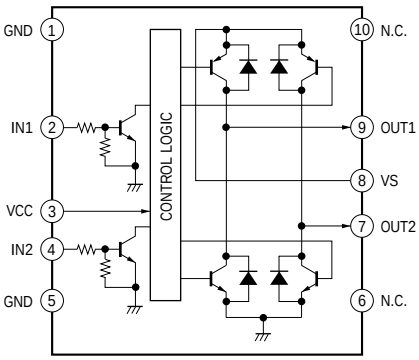
- All capacitors are in µF unless otherwise noted. pF: µµF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and 1/4 W or less unless otherwise specified.
- B + : B+ Line.

• **IC Block Diagrams**

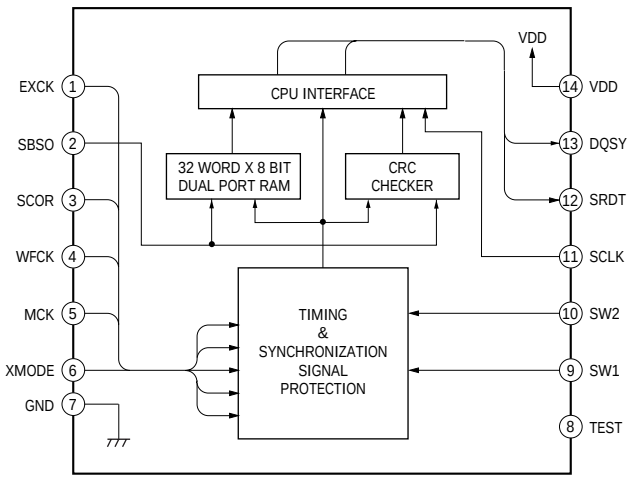
IC1 CXA1791N-T4 (SERVO BOARD)



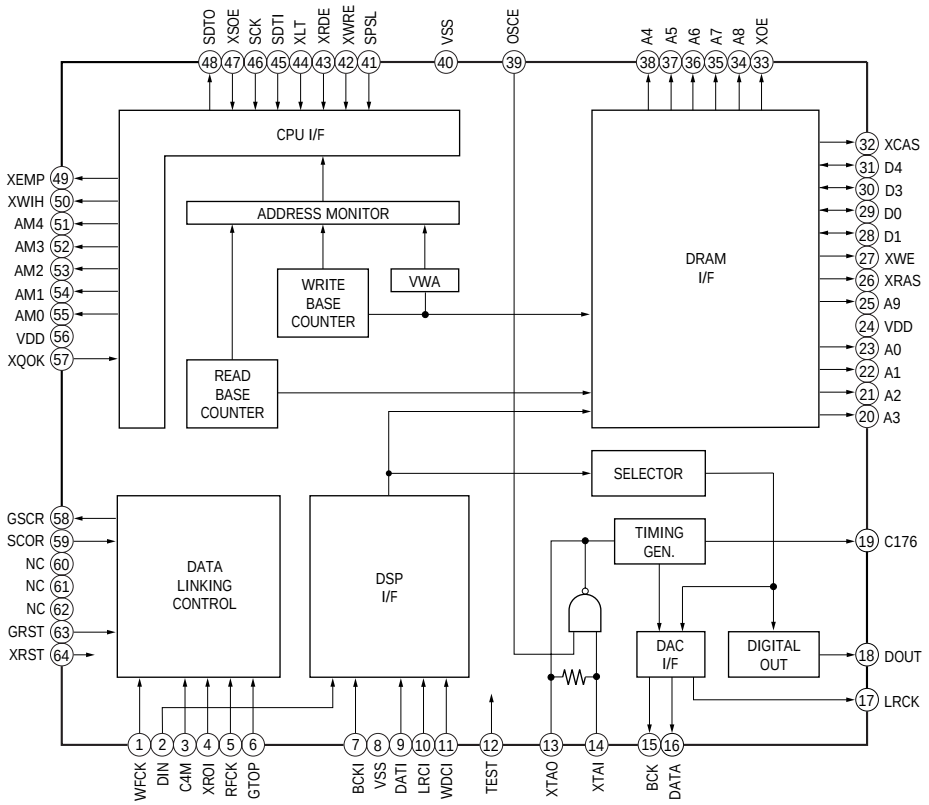
IC6 LB1638MTP-T1



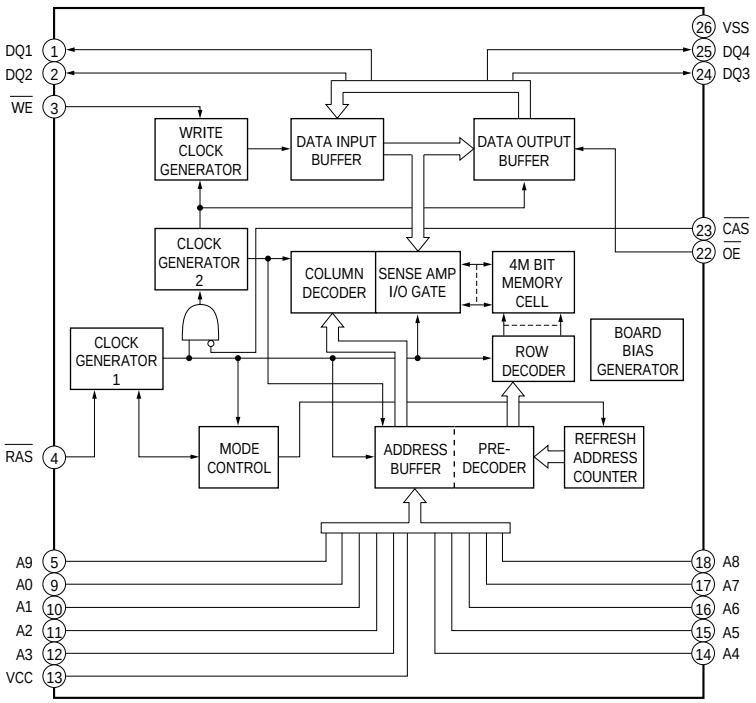
IC551 LC89170M-TLM



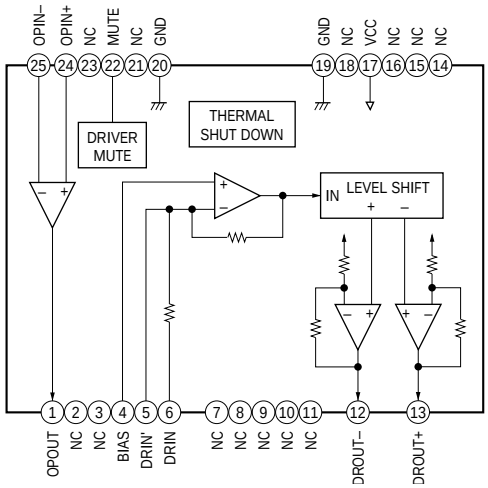
IC2 CXD2522R-T6



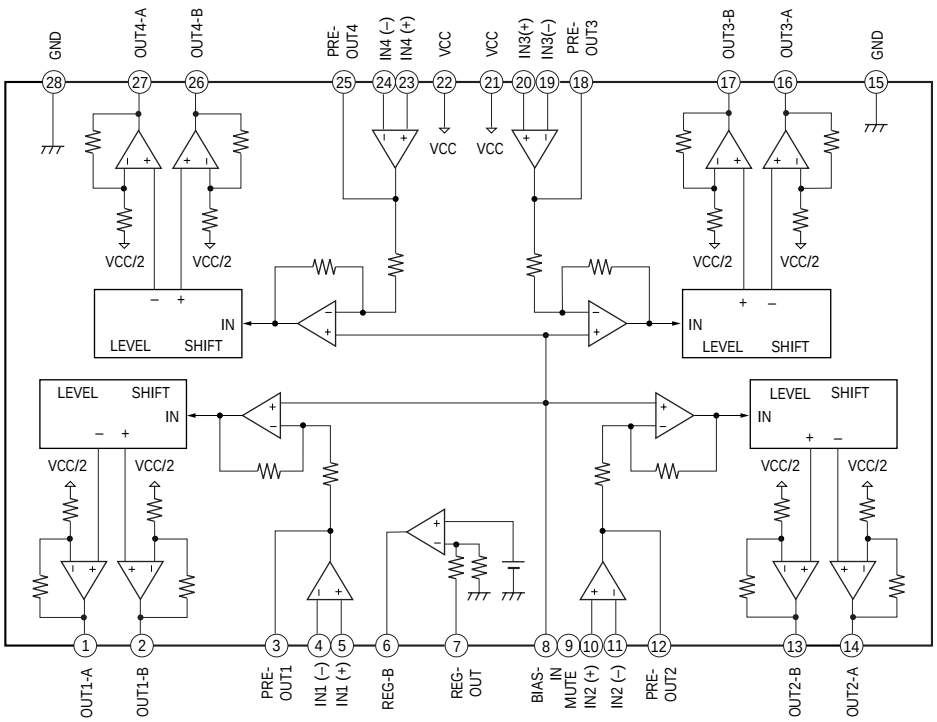
IC4 MB814400C-70PFTN (SERVO BOARD)



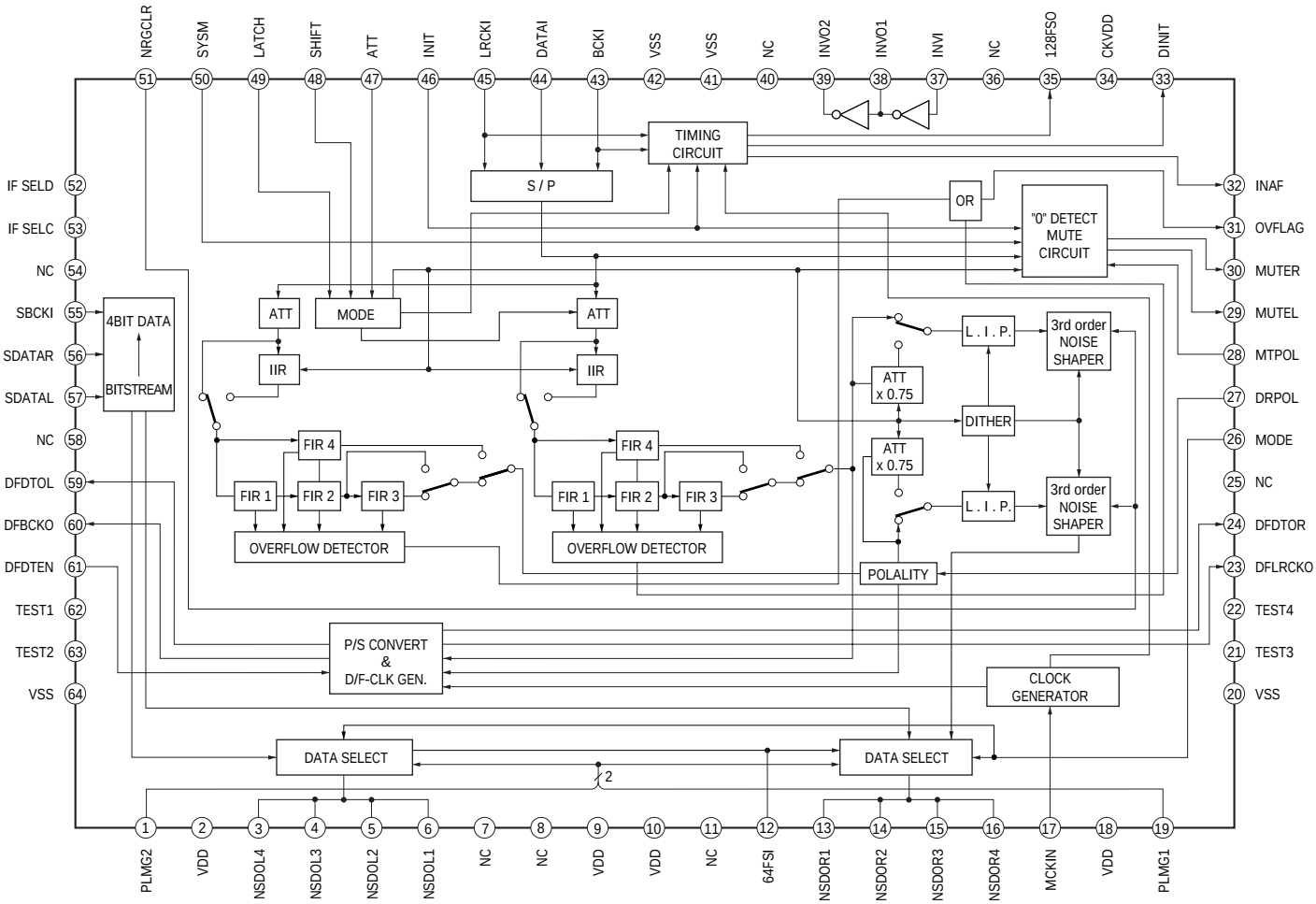
IC601 BA6195FP-YT2



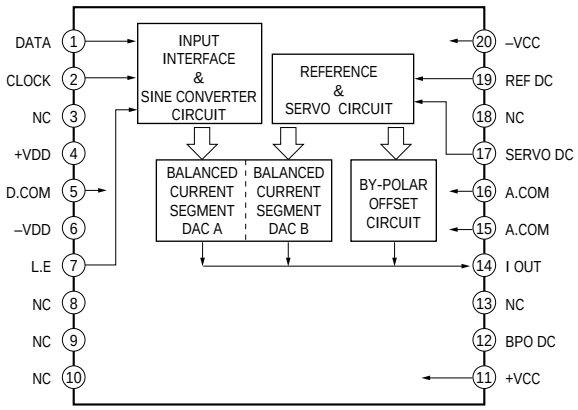
IC7 BA6797FP-E2



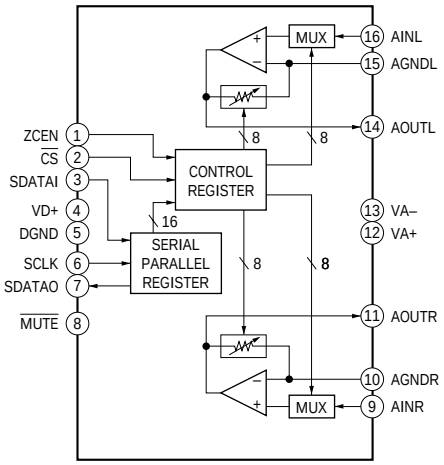
IC1 CXD8679Q (MAIN BOARD)



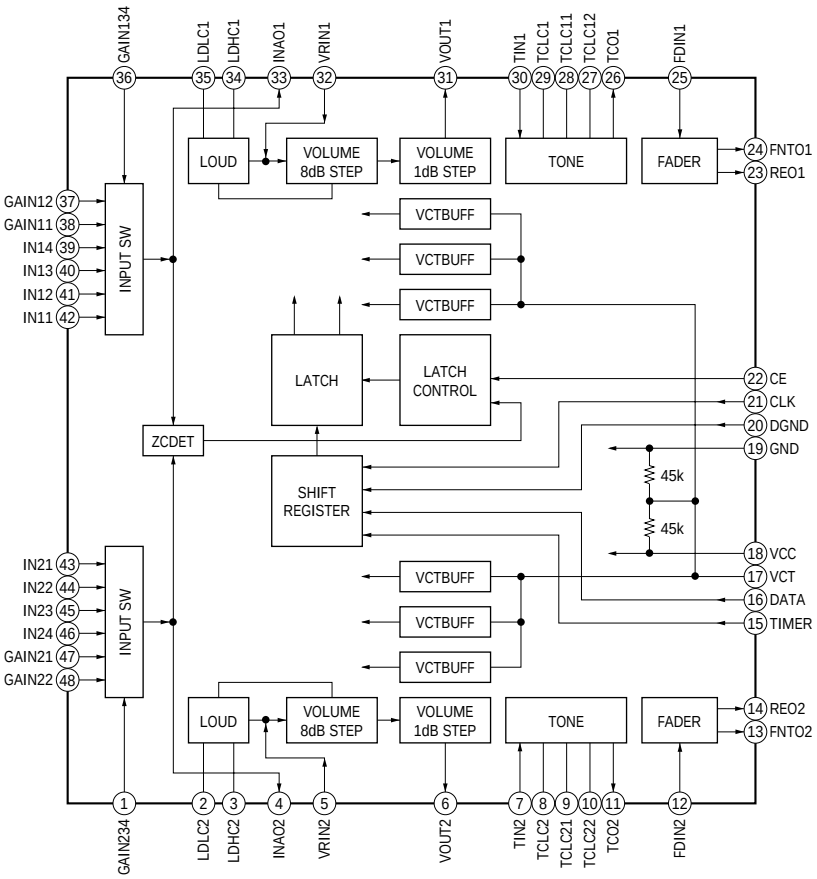
IC3, 4 PCM1702U-J (MAIN BOARD)



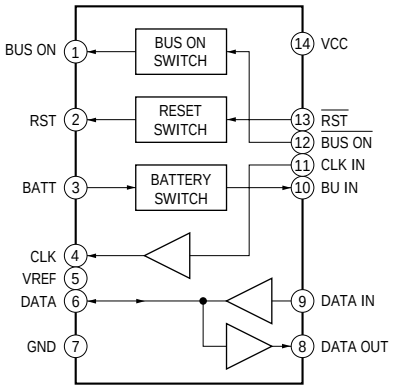
IC103, 104 CS3310-KSR



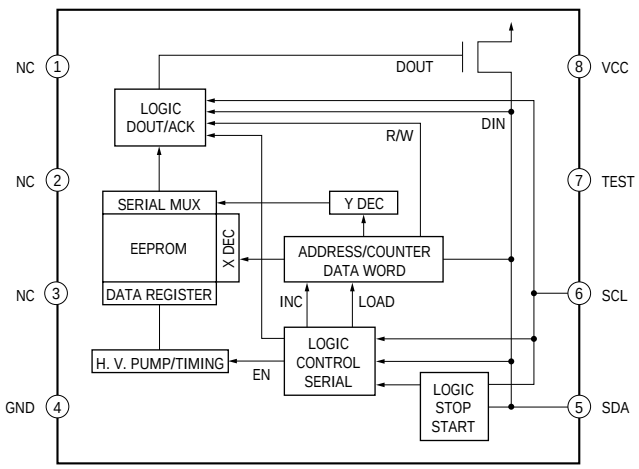
IC102 CXA1946BR



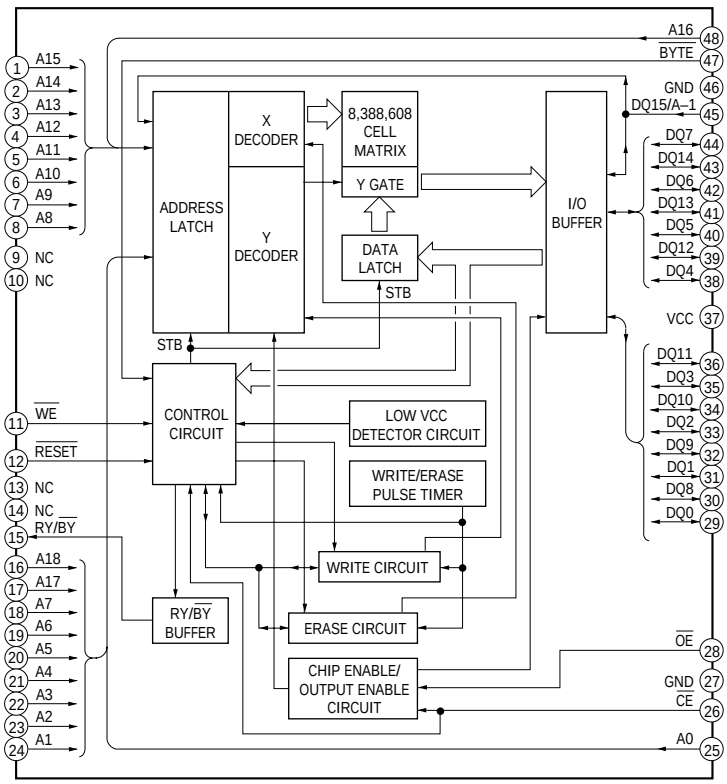
IC302 BA8270F-E2



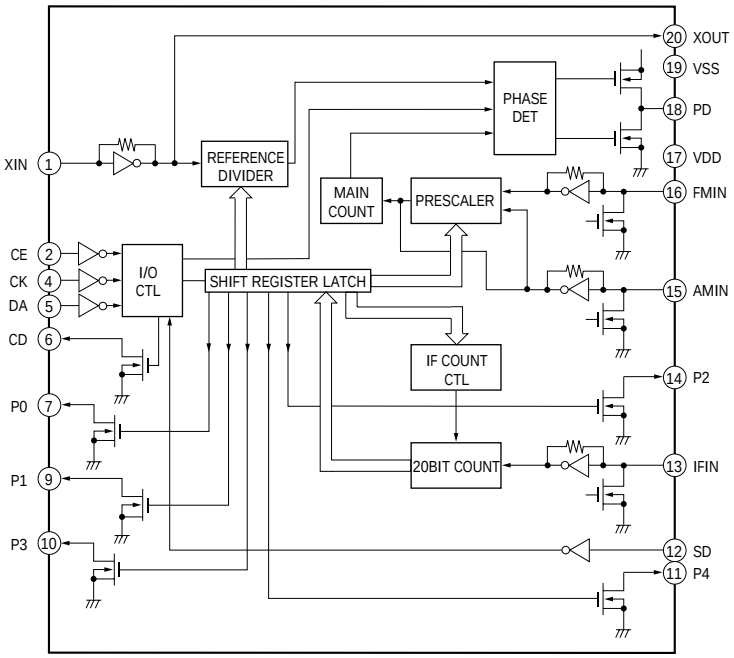
IC303 AT24C16N-10SI-TR



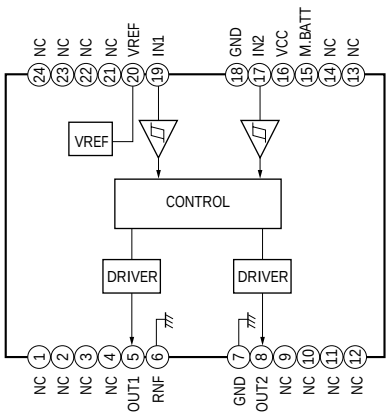
IC503 MBM29F800BA-70PFTN97



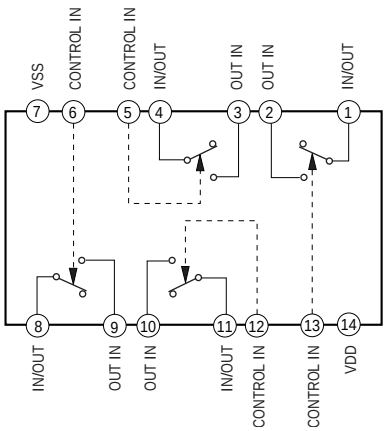
IC721 BU2624FV-E2



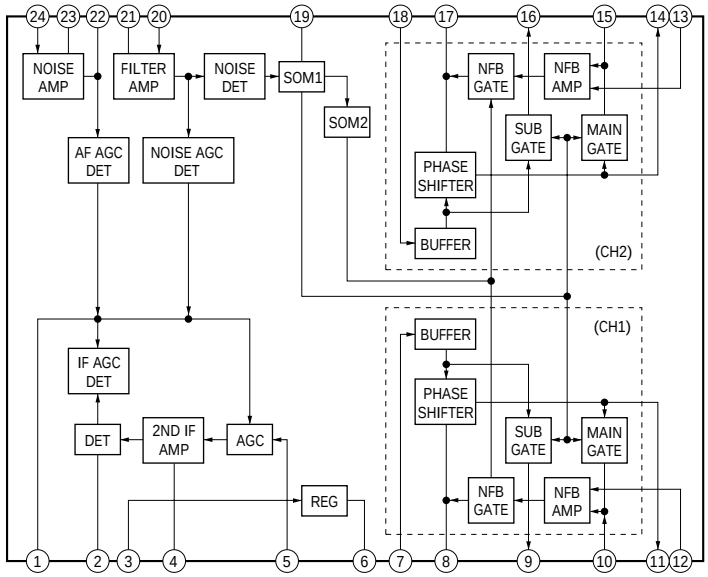
IC600 BA6285FP-E2



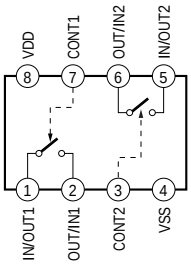
IC761 μPD4066BG



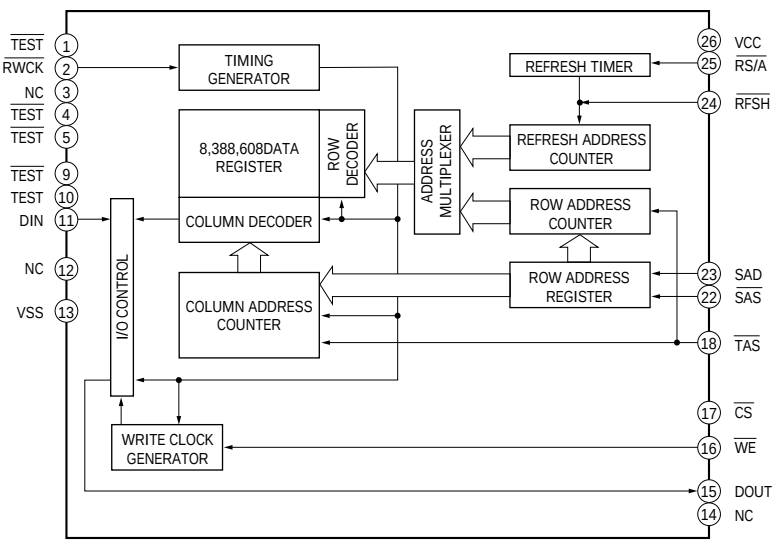
IC851 TA2051FN(EL)



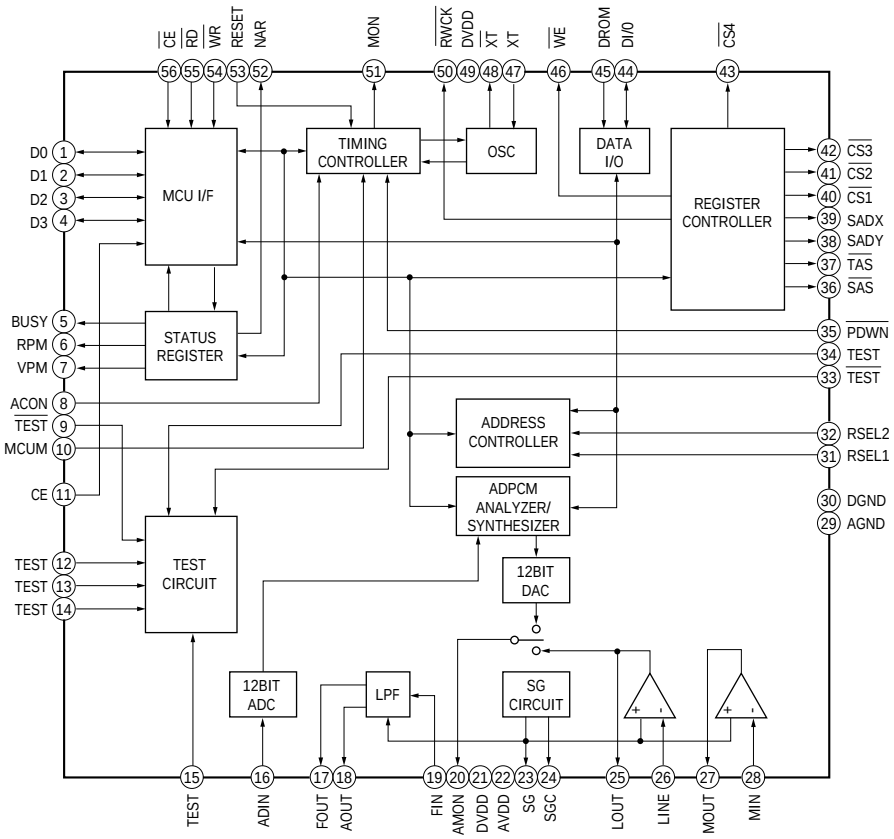
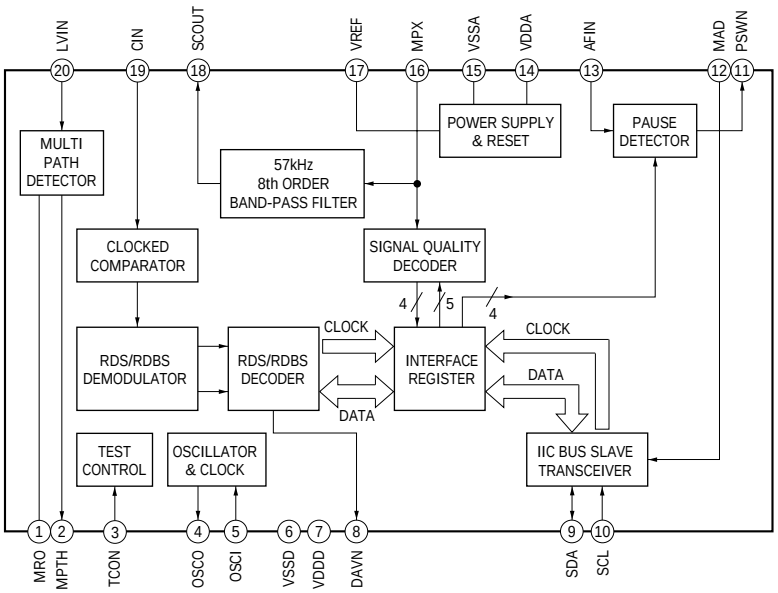
IC722, 941 TCW66FU



IC921 MSM6685JSDR1



IC901 MSM6688GS-2K



IC951 SAA6588